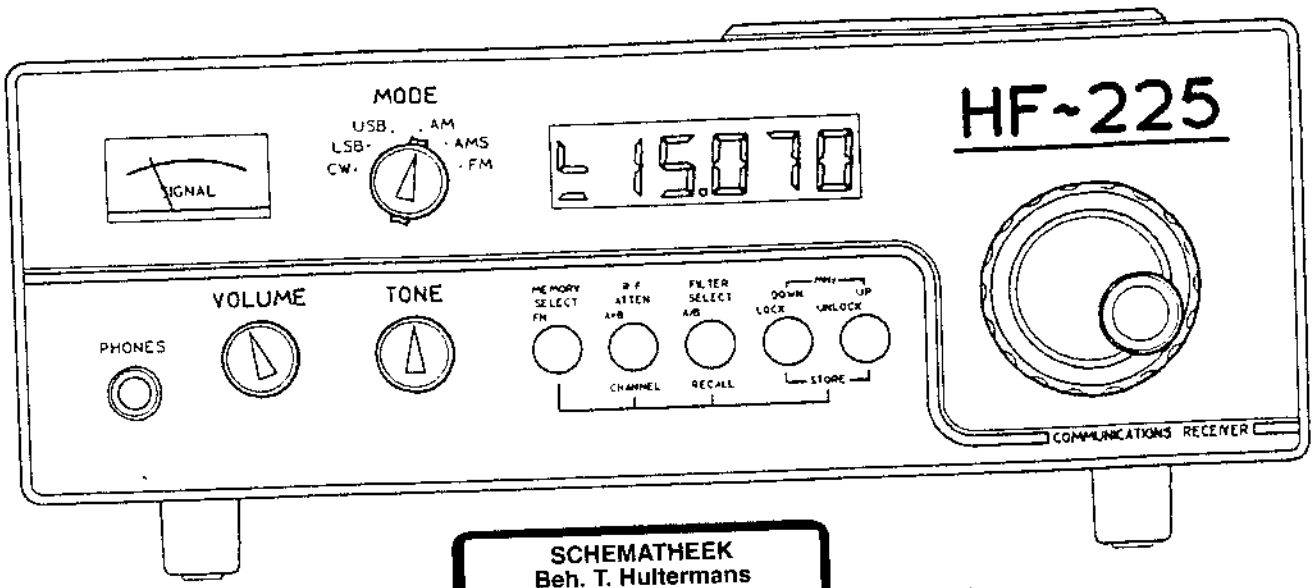
HF-225 General Coverage Receiver.

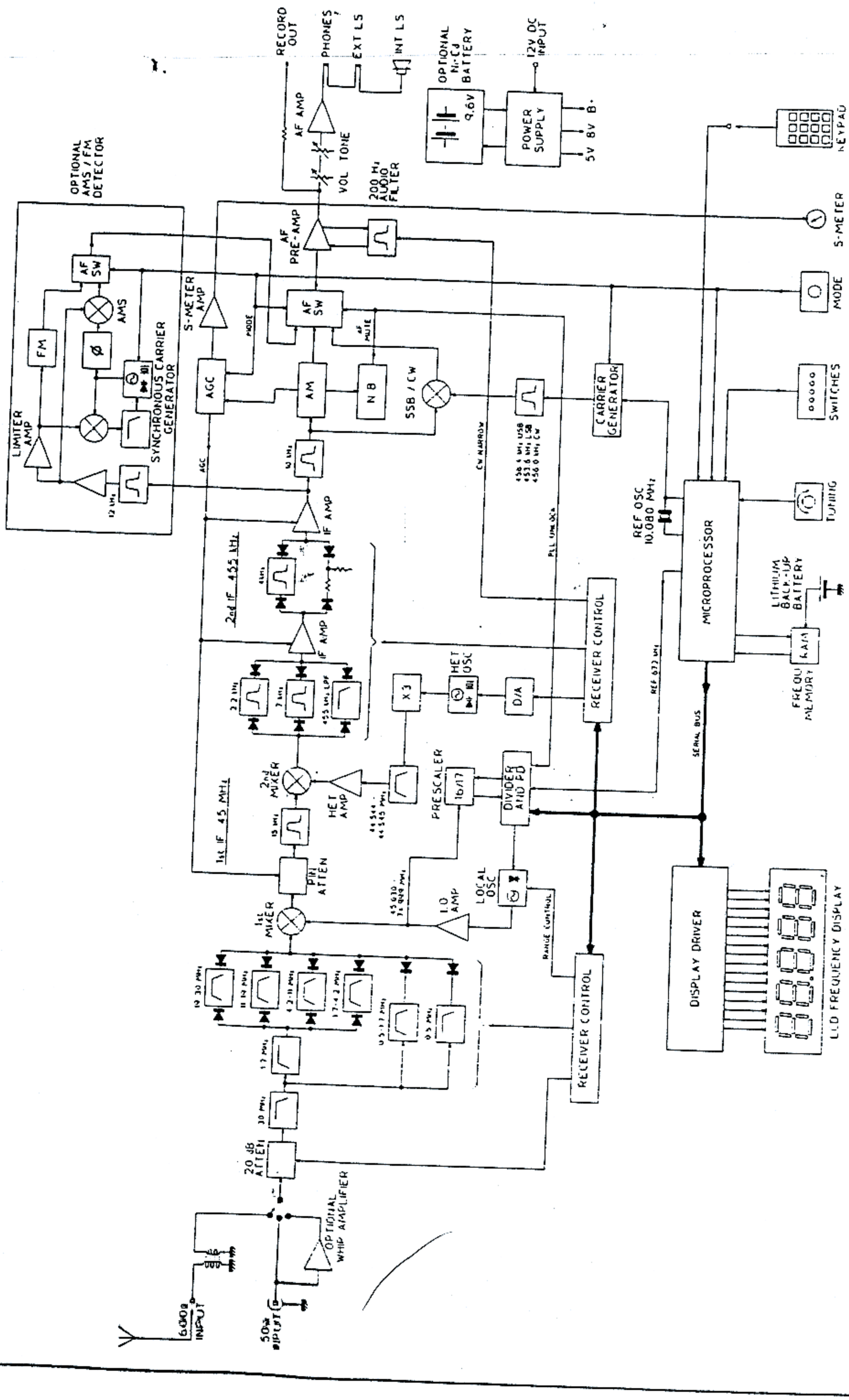
Technical Manual.



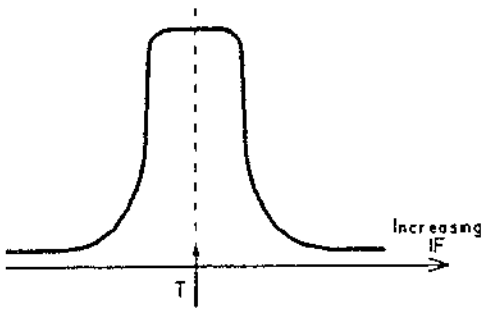
Contents.

Bentley Bridge
Chesterfield Road
Matlock, Derbyshire.
Printed in England. M02-2251

HF-225 BLOCK DIAGRAM

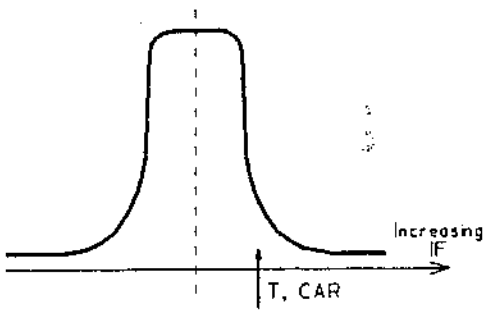


The following diagrams show the relationship between tuned frequency, IF filter centre frequency and carrier reinsertion frequency for each mode.



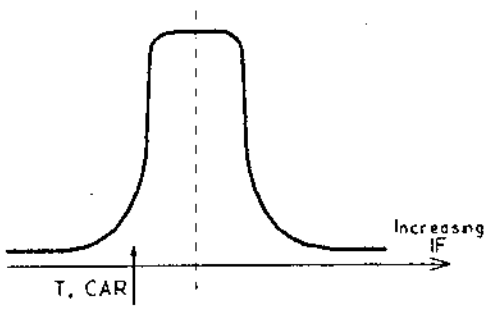
AM and FM modes:

Tuned frequency (T) in centre of filter passband.



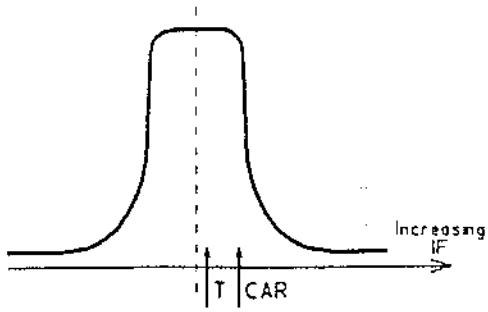
USB mode:

Tuned frequency (T) offset by -1.4 kHz.
Carrier reinsertion (C) offset by +1.4 kHz.



LSB mode:

Tuned frequency (T) offset by +1.4 kHz.
Carrier reinsertion (C) offset by -1.4 kHz.



CW mode:

Tuned frequency (T) offset by -200 Hz.
Carrier reinsertion (C) offset by +1.0 kHz.

1.1 RF preamplifier.

The RF preamplifier is only present when the whip antenna option (W-225) is installed. It offers a high input impedance to give good results at low frequencies with the capacitive load of a whip or a short wire aerial. The JFET input stage, Q1, acts as a source follower to drive the low input impedance of the second bipolar stage, which gives some 10 dB of gain. Transformer T1 provides emitter current feedback to give good linearity, and matches the collector circuit to the 50 ohm input of the receiver.

1.2 Input attenuator and band-pass filters.

Signals from the aerial input of the receiver first pass through the relay-switched attenuator formed by R1 / R2 / R3. The attenuator is bypassed if RL1 is closed, or gives about 20 dB signal reduction if RL2 is closed. Frequencies above 30 MHz are attenuated by the low-pass filter L1 / L2 / C1 / C2 / C3, then signals below 1.7 MHz are separated by the duplexer L21 / L22 / C25. For frequencies above 1.7 MHz, the signal passes through one of four band-pass filters, covering 1.7 to 4.2 MHz, 4.2 to 11 MHz, 11 to 19 MHz and 19 to 30 MHz. Frequencies below 500 kHz have a separate low-pass filter L25 / L26 / C29. These filters all help to reduce spurious mixing effects caused by strong signals outside the frequency band being received.

The appropriate filter is switched into circuit by diodes at the input and output. The control system drives one filter select line low (to ground) whilst holding the others at B+ (about 11V), causing one pair of diodes to conduct, with the remainder reverse-biased. Frequencies below 1.7 MHz are selected only at the output of the filters, and D10 is present to prevent attenuation of signals below 500 kHz by the 0.5 to 1.7 MHz duplexer section. Current for the filter switching diodes first passes through one of the attenuator relay coils, selected by Q5 or Q6.

1.3 1st mixer and 1st IF.

An SL6440 integrated circuit, transistor tree mixer is used to convert the RF signal to the first IF at 45 MHz. Transformer T2 provides a balanced signal feed to the mixer, and the balanced output is matched to the crystal filters X1a and X1b by a tuned transformer T3. Tuning adjustment is provided by TC1. In this configuration the mixer provides enough gain to remove the requirement for a separate RF amplifier stage, and offers more than 90 dB of intermodulation-free dynamic range.

AGC is fed back from the detector stage, via current control Q7, to a PIN attenuator diode D15. This controls the gain of the mixer. Mixer operating current is set by D14 and R17, and the stage is fed from the unregulated B+ supply to maximise dynamic range when the receiver is mains powered but to conserve current when battery operated.

1.4 2nd mixer and 2nd IF.

The second IF section is a cascade of three filters, interspersed with two amplifier stages. There are no adjustments in this section. The IF at 455 kHz is produced by the second mixer, which is also an SL6440 IC, but it is operated at a much reduced current compared to the first mixer. The 15 kHz bandwidth of the first IF filter reduces the dynamic range requirement of the second mixer.

The second mixer output is applied directly to the first group of filters; one of three is selected by the control system. Diode switching passes the signal through either the 2.2 kHz filter (X2), the 7 kHz filter (X3), or through a 500 kHz low-pass filter (C63 / C64 / L34) when the appropriate IF filter select line goes to 5V.

Both of the IF amplifier stages are contained in the SL6700 detector IC, Q5. AGC control to these amplifiers is provided within the integrated circuit. A 4 kHz filter (X4) or a direct connection can be placed between the two amplifiers, again controlled by diode switching. Finally a 10 kHz filter (X5) comes after the second amplifier and before the AM and SSB detectors. A 12 kHz filter is used in place of X5 before the FM and synchronous AM detectors.

IF filter selection is as follows:-

Selected IF bandwidth	1st IF Filter	Filter 1	2nd IF Filter 2	Filter 3
2.2 kHz	15 kHz	2.2 kHz	4 kHz	10 kHz
4 kHz	15 kHz	7 kHz	4 kHz	10 kHz
7 kHz	15 kHz	7 kHz	Thru	10 kHz
10 kHz	15 kHz	500 kHz	Thru	10 kHz

1.5 Detectors and AGC system.

The SL6700 IC contains the AM and SSB detectors, the AGC system and an impulse noise blanker. A full-wave envelope detector provides the AM audio output and feeds an IF signal level to the AGC system. The AGC time constant is provided by C86 and C87 in all modes, and additionally C88 is switched in by Q12 in AM mode to provide slower attack and decay. Transistors Q9 and Q10 provide a fast AGC attack for SSB mode, but this is disabled by Q11 during noise impulses and when the local oscillator is tuning between required frequencies. The AGC voltage is used to drive the S-meter after inversion and amplification by a section of Q24. Diode D40 expands the meter scale for large signals, and VR1 is the S-meter mid-point adjustment.

The noise blanker is triggered by noise spikes about 12 dB above the normal IF level. R54 and C84 determine the blanking period, which is about 0.5 ms. The blanking pulse is fed to the audio muting gate via D28.

1.6 Optional detector unit.

The optional FM and synchronous AM detector is based around the MC3357 narrow-band FM IF integrated circuit. This contains limiting amplifiers and a quadrature FM detector along with a squelch circuit - diodes D1 and D2 rectify the output of an active noise filter to produce a voltage representing the level of audio noise. If this exceeds a level preset by the squelch control then the receiver is muted.

In AMS mode, the resonator X3 provides a narrow range VCO to generate a carrier signal. The mixer inside the MC3357 is used to phase-lock this VCO to the incoming signal after it has passed through a limiting amplifier. Trimmer TC1 adjusts the oscillator centre frequency to 455 kHz. The oscillator signal is fed to mixer Q5 after a 90 degree phase shift, so that the mixer can correctly detect an AM signal. The mixer output is filtered by R29 / C28 to remove the IF component leaving the AMS audio signal.

The FM / AMS audio switching is done by Q10, a CMOS switch, whilst Q7 and Q8 provide switched 8V supplies to the detector stages. Logic circuit Q6 controls supply switching, the squelch enable (FMS) and the audio gate (MUT). Transistor Q9 detects if an audio beat-note is present on the output of the phase-detector (indicating that the AMS detector is out-of-lock) and controls the LCK signal to the front panel lock indicator.

1.7 AF stages.

Audio switching between the SSB and AM detectors is carried out by a CMOS switch Q27. SSB audio from the product detector is buffered by Q23 before the switching circuit. Op-amp Q24 amplifies the audio signal and Q22 provides audio muting at this point. A further section of Q24 acts as a second amplifier that can be switched to a band-pass filter by two further sections of switch Q27. This filter has a -6dB bandwidth of about 200 Hz, centred on 800 Hz, and is used for the narrow CW filter.

The preamplifier output is fed to the record out jack at a constant level, and via the volume and tone controls to the AF amplifier and to the loudspeaker. The final amplifier is fed from the unregulated B+ supply to maximise available audio output power. The tone control is arranged as a bridge circuit giving either treble cut or bass cut.

1.8 Power supply.

Four supply rails are used in the receiver:-

5 Volts for the logic and control system, 455 kHz IF amplifiers and signal switching.

8 Volts for the 45 MHz IF stages, the PLL system and HET oscillator, and the audio preamplifier.

6 Volts specially regulated and smoothed for the local oscillator and buffer amplifiers. (Derived from the 8V supply via Q21).

An unregulated supply between 9V and 15V (B+) for the first mixer and the audio amplifier.

The 8V and 5V supplies are provided by regulators Q32 and Q33 from the B+ supply. A low voltage drop regulator (LM2930 series) is used for the 8V rail to give a stable supply under battery operation when B+ may only be 9V. A large part of the receiver's current consumption is on the 5V supply, and the display illumination LED's are connected between B+ and 5V to take advantage of the voltage drop across the regulator. Transistor Q202 maintains a constant LED brightness.

The battery option B-225 adds a 9.6V rechargeable NiCd battery, which powers the receiver when there is no plug in the DC power input jack. If the receiver is operating from an external supply, the batteries are maintained with a small trickle charge of a few mA via D45 and R141. When the receiver is switched off, the cells are reconnected as two 4.8V batteries, and the charging current increases to about 150 mA for each cell. Resistors R140 and R141 control charging current.

Diode D43 provides protection against a reverse-polarity supply connection, but care should be taken that the normal supply does not exceed 16V. Current consumption is 200 to 250 mA in normal use.

2) PLL section.

2.0 Frequency configuration.

The PLL system and two other signal sources grouped in this section produce the local oscillator (LO), heterodyne (HET) and carrier (CAR) signals that are fed to the IF mixers. There is no signal interconnection between these sources, but their frequencies are controlled together in order to tune the receiver.

The following frequency relationships apply:-

Received frequency = <LO> - <HET> - 455 kHz in AM and FM modes.

Received frequency = <LO> - <HET> - <CAR> in SSB and CW modes.

2.1 Carrier generator.

The carrier generator circuit is split into two sections - a programmable digital divider which is situated on the control unit PCB, and a filter and amplifier which is on the main unit PCB. The programmable divider takes its input from the 10.080 MHz reference oscillator in the microcontroller, Q205. When a carrier signal is needed (in CW, LSB and USB modes) Q208 divides the reference frequency by four to give 2.52 MHz which is fed to programmable counter Q209. The counter division ratio is controlled by the mode setting:-

Selected Mode	Division ratio	Counter o/p frequency	Selected harmonic	CAR frequency
CW	210	12.000 kHz	38 th	456.000 kHz
LSB	250	10.080 kHz	45 th	453.600 kHz
USB	254	9.9213 kHz	46 th	456.378 kHz

The output from the programmable divider is a stream of short pulses, containing many harmonics of the fundamental frequency. This pulse stream is fed through a 4 kHz bandwidth ceramic filter which selects one harmonic near to 455 kHz. This is then amplified and fed to the product detector.

2.2 Heterodyne oscillator.

The heterodyne oscillator, Q19 / X7, is a fundamental mode crystal oscillator running at about 14.848 MHz. The diode D36 in the drain of FET Q19 is operated in its non-linear region and produces strong harmonics of the fundamental frequency. The third harmonic at 44.545 MHz is selected by tank circuit TC4 and L42, amplified by Q4, and fed to the second mixer.

The oscillator frequency is adjusted by TC3 and also by the bias voltage on varicap diode D30. A change of about 0.6V in bias will move the oscillator frequency by 330 Hz, resulting in a 1 kHz change of HET frequency. The bias voltage is derived from a section of the Q24 op-amp which acts as a current-to-voltage converter driven through an R - 2R - 4R ... resistor chain (R85 to R91) from a 7-bit control register. The HET frequency can be controlled in 128 steps across its 1 kHz range, each step being nominally 7.8 Hz.

Variable resistor VR2 adjusts the span of the HET oscillator tuning. Component values in the current-to-voltage converter are chosen so that the setting of VR2 has little effect at the highest bias voltage (corresponding to maximum HET frequency and minimum tuned frequency), allowing VR2 and TC3 to be adjusted independently.

2.3 Local oscillator.

The local oscillator, Q18, is a wide range VCO tuning from 45 MHz to 75 MHz. A JFET is used as the gain element to provide a low-noise signal which is buffered by Q16 / Q17 then fed to the first mixer and the PLL system divider. The oscillator is tuned by varicap diode D29 controlled from the PLL system. Four frequency ranges are available depending on the control voltages on LO1, LO2 and LO3. PIN diodes D31, D32 and D33 select the required inductance value of oscillator coil T4.

Coils and frequency ranges are selected as follows:-

Tuning range (MHz)	LO frequency (MHz)	Select lines LO1	LO2	LO3
0.030 to 4.999	45 to 50	Low	Low	High
5.000 to 10.999	50 to 56	High	Low	High
11.000 to 18.999	56 to 64	Low	High	High
19.000 to 29.999	64 to 75	Low	Low	Low

2.4 PLL system.

The PLL system controls the frequency of the local oscillator using a crystal-derived reference of 672 kHz from the control system. All of the functional blocks of the PLL system are contained in Q29 but a prescaler, Q28, is also required to reduce the local oscillator frequency so that Q29 can operate correctly. Q28 is a dual-modulus prescaler, and can divide by 16 or 17 under the control of Q29 in a pulse-swallowing counter. This counter is arranged as a programmable divider, where the division ratio can be controlled by the receiver's microcontroller.

Both the LO signal and the reference are divided down to 1 kHz and applied to phase detector circuits in Q29. When the phase error is large, a linear digital phase detector can correct the loop error quickly. As the phase error becomes small, the digital detector becomes inactive and an analogue sample-and-hold detector is used instead. This can only correct small phase errors, but offers much better residual noise performance than the digital detector. When the digital detector operates, the out-of-lock output from Q29 goes high, muting the receiver audio.

Both phase detector outputs go to an active integrating loop filter formed by op-amp Q25. The output from this is further filtered by R81 / C115 and then controls varicap diode D29 in the oscillator circuit. To increase the available voltage swing on the tuning diode, its cathode is held at 2 volts below ground. The negative potential is derived from a charge pump C129 / D37 / D38 / C130, driven by an output at 14 kHz from the PLL IC, Q29.

3) Control section.

3.0 Microcontroller and control program.

At the centre of the control system is the microcontroller Q205. This integrated circuit contains all of the elements of a microprocessor system - program memory (ROM), data memory (RAM), a central processing unit and input and output ports. With the exception of the clock oscillator and the REF output at 672 kHz, all lines into and out of the microcontroller are in a static condition unless the receiver's controls are operated, so the signals radiated by the control system are kept at a very low level.

The microcontroller chip contains a control program specific to the HF-225 receiver. This program provides an interface between the operator and the receiver's tuning and filter selection systems, and also provides additional features such as frequency memories. The program accepts commands from the tuning encoder, the function buttons, the mode switch and the remote keypad, and in turn controls the display, the input filters, the RF attenuator, the IF and audio filters, the PLL system and the heterodyne oscillator.

When the control system is in an idle condition, with no controls being operated, the control program remains in a monitoring loop looking for any changes in the controls. If any control is moved, the program detects this and modifies its internal status to suit. This may involve just changing internal memory values, or it may require data to be sent to the display or the receiver control registers. There are four subprograms in the monitoring loop, dealing with the tuning knob, the mode switch, the function buttons and the external keypad.

As an example of the operations performed by the control program, consider the action of the program in response to rotation of the tuning knob.

Tuning encoder rotation is detected:-

Establish direction of rotation (up/down).

Establish speed of rotation (fast/slow).

Check mode selected and look-up tuning rate from internal table.

Increase or decrease stored frequency value by tuning rate value.

Check the new tuning value against the operating frequency limits and inhibit tuning if these are exceeded.

If the kHz digits have changed, convert the frequency value into 7-segment digits and send this data to the display.

Select the appropriate input filters and local oscillator frequency range.

Convert the frequency value into binary form suitable for programming the PLL synthesizer and add an offset value depending on the mode selected.

Send the new frequency information to the heterodyne oscillator and, if they require reprogramming, to the PLL and the receiver control registers.

Store the new frequency value in external non-volatile memory.

Check the tuning encoder for further rotation, and either repeat this sequence or return to the monitoring loop.

All tuning of the receiver is done in terms of fine-tune steps. Each 1 kHz of tuning range is divided into 128 steps, so each step is approximately 8 Hz. One complete rotation of the tuning encoder generates 200 pulses, and each of these pulses will change the frequency by a preset number of steps. The number depends on the tuning rate and the mode selected according to the following table:-

Receiver Mode	Tuning increments (steps of 7.8 Hz)	
	Slow tuning rate	Fast tuning rate
CW, LSB, USB	1	12
AM	6	64
AMS	1	1
FM	16	64

The fast or slow tuning rates are selected according to the rate at which pulses come from the tuning encoder. Note that in practice the fast tuning rate will not be as fast as indicated in the table because some pulses from the encoder will be missed by the control program (when it is involved in other tuning operations), therefore rapid rotation of the tuning knob usually results in a mixture of fast and slow tuning rates.

As each new kHz frequency is tuned the control program establishes which input filter to select and which local oscillator frequency range to select. The same part of the program also checks the frequency range limits, which are normally 30 kHz minimum and 29999 kHz maximum. The limits may be restricted further to frequencies above 148 kHz by insertion of JP1 on the control unit, which takes an input port line to ground and modifies the program operation. Frequencies outside the limits, whether derived from the memories or entered from the external keypad, are converted to the nearest limit frequency.

Filter and oscillator ranges are summarised below:-

Receiver frequency		Input filter	Oscillator range
(Low limit)	30 kHz	1	0
(Low limit *)	148 kHz	1	0
	499 kHz	1	0
	500 kHz	2	0
	1699 kHz	2	0
	1700 kHz	3	0
	4199 kHz	3	0
	4200 kHz	4	0
	4999 kHz	4	0
	5000 kHz	4	1
	10999 kHz	4	1
	11000 kHz	5	2
	18999 kHz	5	2
	19000 kHz	6	3
(High limit)	29999 kHz	6	3

* Restricted range with JP1 installed.

3.1 Controls.

The front panel controls connect to the microcontroller through an 8-bit input port, P1. The five function buttons each pull an input line down to ground when pressed; there is a pull-up resistor to 5V inside the microcontroller chip. Tuning knob rotation is detected by a mechanical shaft encoder, which generates two streams of pulses which differ in phase. The controller is able to establish the speed and direction of tuning from these two signals after pulse shaping and glitch removal by Q207.

The rotary mode switch controls the receiver state by switching several supply lines (all at 5V) feeding the carrier generator, the AGC system and the detector audio switching. Three of these lines are sampled by the microcontroller through its flag inputs T0, T1 and INT so that tuning rates and frequency offsets can be established. Mode supplies are switched as follows:-

Mode	Supply line state						Flag state		
Selected	SSB	USB	FM	AMS	AM	CW	T0	T1	INT
CW	5V	0V	0V	0V	0V	5V	1	0	1
LSB	5V	5V	0V	0V	0V	0V	1	1	0
USB	5V	0V	0V	0V	0V	0V	1	0	0
AM	0V	0V	0V	0V	5V	5V	0	0	1
AMS	0V	5V	0V	5V	0V	0V	0	1	0
FM	0V	0V	5V	0V	0V	0V	0	0	0

3.2 Frequency memory.

Frequencies stored in the receiver's memories are not held within the microcontroller, but are stored in RAM chip Q204, a CMOS device with its supply maintained by a lithium battery when the receiver is switched off. The tuned VFO frequency is also stored in this RAM so that the receiver can resume operation on its previous frequency at switch-on.

Inside the receiver, frequencies are stored in the form of separate decimal digits for the kHz part (5 digits) and as a 7-bit binary value for the fine tune part (fractions of kHz). The external frequency memory chip is 4-bits wide by 256 locations; each frequency uses eight locations - five for the kHz digits, two for the fine tune value and one unused location. There is room in the memory for 32 frequency entries, but only 31 are used for the 30 memories and the VFO frequency.

Q204 is not attached to the microprocessor bus, but is controlled via an 8-bit output port (for the address information) and a 4-bit wide bidirectional port (for data). The data port is shared with the external keypad. The RAM is controlled by three other lines; read and write strobes from the microcontroller which pulse momentarily low to transfer data to or from the RAM, and a power-down line from voltage detector Q201 which disables the RAM when power is turned off and prevents data corruption.

3.3 Display.

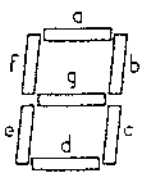
The liquid crystal frequency and function display is driven from a dedicated controller Q206. The LCD segments turn on when a voltage exists between the segment line and the backplane or common. It is important that there is no residual current flow through an LCD, so the segments are driven with a low frequency AC supply produced inside Q206 by oscillator R224 / C212. The backplane connection is fed with a square wave at about 60 Hz, and blank segments are fed with an identical signal. Lit segments are fed with a signal in antiphase to the backplane. The display used is a negative image one, so it is normally all black, and segments become clear when energised.

Segment data is transferred from the microcontroller to the display driver by a two line serial bus; DATA and CLOCK. Data transfer commences when the data line goes high and the clock line pulses low, then the state value of each segment is placed on the data line and the clock line pulsed low again for each segment. Transfer is complete when 35 bits of data have been sent, and then the display will be changed to the new configuration. Further clock pulses will be ignored until the data line goes high again.

Display driver serial data format:-

Bit 0 (start)	always high (1)		Bit 18	digit 5	seg g
Bit 1	memory flag		Bit 19	digit 4	seg b
Bit 2	decimal point		Bit 20		seg a
Bit 3	digit 2	seg e	Bit 21		seg f
Bit 4		seg d	Bit 22		seg g
Bit 5		seg c	Bit 23	digit 3	seg b
Bit 6	digit 3	seg e	Bit 24		seg a
Bit 7		seg d	Bit 25		seg f
Bit 8		seg c	Bit 26		seg g
Bit 9	digit 4	seg e	Bit 27	digit 2	seg b
Bit 10		seg d	Bit 28		seg a
Bit 11		seg c	Bit 29		seg f
Bit 12	digit 5	seg e	Bit 30		seg g
Bit 13		seg d	Bit 31	digit 1	seg b
Bit 14		seg c	Bit 32		seg c
Bit 15		seg b	Bit 33		seg a,d,e,g
Bit 16		seg a	Bit 34	always low (0)	
Bit 17		seg f	Bit 35	always low (0)	

Digit 1 = 10's MHz (Only blank, 1 or 2)
Digit 2 = units MHz
Digit 3 = 100's kHz
Digit 4 = 10's kHz
Digit 5 = units kHz

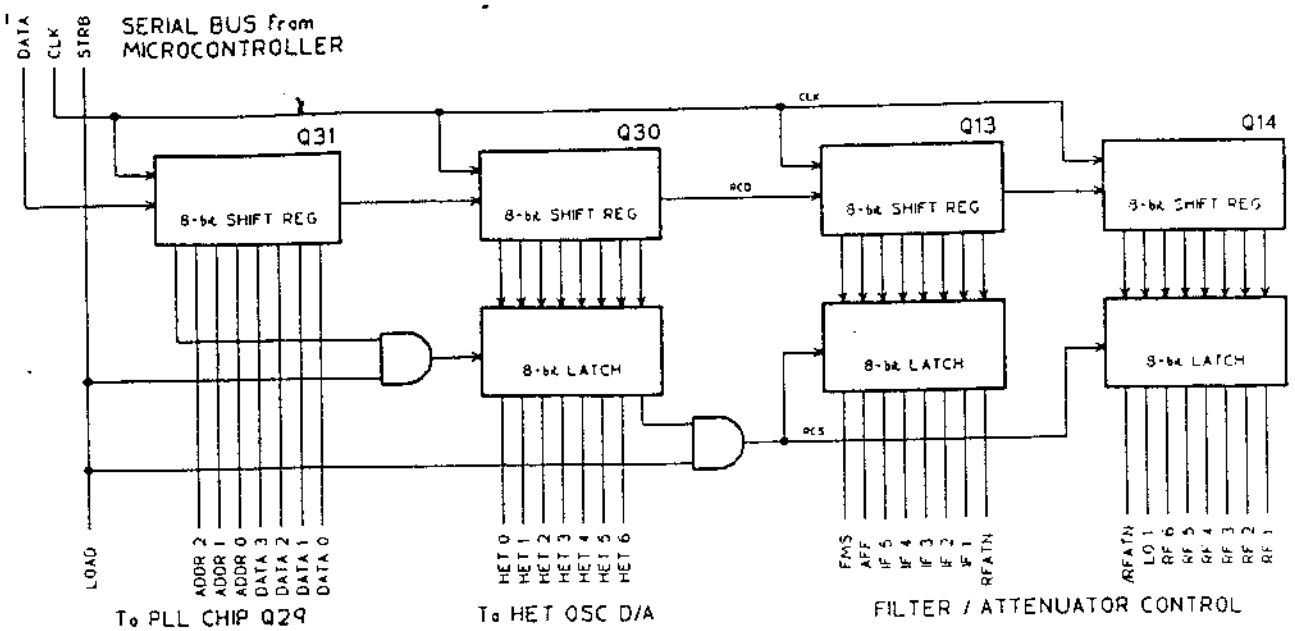


The AMS LOCK indicator segments of the display are not controlled from the display driver chip, but are driven from the exclusive-or gate Q207. This is driven from the LCD backplane signal and provides a true or inverted feed to the two L segments depending on the logic state of the LCK signal from the detector board.

3.4 Receiver interface.

The switching functions within the receiver are controlled via a three line serial bus from the microcontroller, which sends data to registers located on the main receiver circuit board. The three lines (CLK, DATA and STRB) are filtered near to the point of entry to the main unit by L networks to prevent low-level spurious signals from entering the receiver control lines.

The serial data is converted into steady-state signals for receiver control by a series of cascaded shift registers - Q13, Q14, Q30 and Q31 are each 8-bit registers. Because not all of the control lines need to change when the receiver is tuned, the shift register can be split into three sections, effectively limiting its length to 8, 16 or 32 bits. To set the control registers, a data stream of the appropriate length is sent from the microcontroller, each data bit separated by a clock pulse (the CLK line goes momentarily low) The end of the data stream is marked by the STRB line pulsing high. Note that the CLK signal is shared between the display driver and the receiver control, so there will be spurious data and clock signals fed into the registers; only the data stream before a STRB pulse has any effect on the receiver.



Receiver control shift-register arrangement.

The format of receiver control data is shown below:-

Format 1: 8-bit data, PLL register load.

Bit 0 (start)	PLL register data bit 0 (lsb)
bit 1	PLL register data bit 1
bit 2	PLL register data bit 2
bit 3	PLL register data bit 3 (msb)
bit 4	PLL register address bit 0
bit 5	PLL register address bit 1
bit 6	PLL register address bit 2
bit 7	ZERO to select 8-bit shift register length

Format 2: 16-bit data, HET oscillator tune.

Bit 0 (start)	ZERO to select 16-bit shift register length
bit 1	HET tune data bit 6 (msb)
bit 2	HET tune data bit 5
bit 3	HET tune data bit 4
bit 4	HET tune data bit 3
bit 5	HET tune data bit 2
bit 6	HET tune data bit 1
bit 7	HET tune data bit 0 (lsb)
bit 8	ZERO
bit 9	ZERO Null command to PLL chip
bit 10	ZERO (register = 0)
bit 11	ZERO (data = 0)
bit 12	ZERO
bit 13	ZERO
bit 14	ZERO
bit 15	ONE to select 16-bit shift register length

Format 3: 32-bit data, Filter selection.

Bit 0 (start)	Input filter 1 select	ONE for Fr < 500 kHz
bit 1	Input filter 2 select	ONE for 500 kHz to 1.7 MHz
bit 2	Input filter 3 select	ONE for 1.7 to 4.2 MHz
bit 3	Input filter 4 select	ONE for 4.2 to 11 MHz
bit 4	Input filter 5 select	ONE for 11 to 19 MHz
bit 5	Input filter 6 select	ONE for Fr > 19 MHz
bit 6	Local Osc range 1 select	ONE for 5 to 11 MHz
bit 7	RF attenuator control	ZERO to attenuate
bit 8	RF attenuator control	ONE to attenuate
bit 9	IF filter 1 select	ONE for 10 kHz
bit 10	IF filter 2 select	ONE for 4 kHz and 7 kHz
bit 11	IF filter 3 select	ONE for 2.2 kHz
bit 12	IF filter 4 select	ONE for 2.2 kHz and 4 kHz
bit 13	IF filter 5 select	ONE for 7 kHz and 10 kHz
bit 14	Audio filter select	ONE for 200 Hz audio filter
bit 15	FM squelch control	ONE for squelch bypass
Bit 16	ONE to select 32-bit shift register length	
Bits 17 to 31	As format 2, bits 1 to 15	

The PLL synthesizer chip Q29 is programmed on a register by register basis, each one of eight registers selected by the three address lines. To change the PLL frequency, seven of the registers need reprogramming, the remaining register is programmed only when the receiver is first switched on. The programmable divider in Q29 is set with a 17-bit binary number, which is the PLL frequency in kHz.

PLL chip register contents are as follows:-

Register	Address bits			Data bits				
	A2	A1	A0	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	Used as Null command
1	0	0	1	N3	N2	N1	N0	
2	0	1	0	0	0	0	0	Loaded at switch-on
3	0	1	1	N7	N6	N5	N4	
4	1	0	0	0	N10	N9	N8	
5	1	0	1	N14	N13	N12	N11	
6	1	1	0	0	0	N16	N15	
7	1	1	1	0	1	1	1	End programming sequence

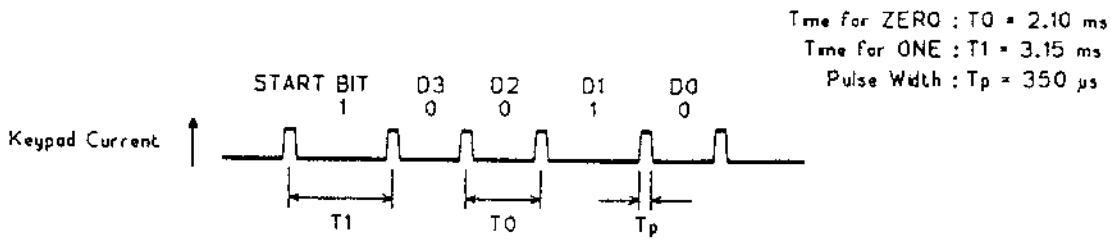
3.5 External keypad.

The remote keypad, K-225, uses a two-wire serial link to communicate with the receiver. Key depressions are converted into an asynchronous PPM (pulse position modulation) data stream by integrated circuit Q1 - each key is uniquely represented by a 5-bit word which is sent repetitively whilst the key is held down. Power for the keypad unit is also sent down the two wires, and data is transmitted by current modulation of this supply. Transistor Q4 is switched by the data output of Q1 to achieve this.

The keypad unit current passes through R204 on the control unit board, and with Q203 this serves to recover the PPM data. Q203 is normally turned off, but when the keypad is operated, charge pump C202 / D203 provides bias to switch the transistor on except for a short period during each data pulse. The PPM data is presented to the microcontroller on P20, one of the RAM data lines. Data stream decoding is done by software within the microcontroller. When a key on the keypad is released, Q203 turns off after a short delay allowing normal RAM data bus operation.

Each key code is transmitted as a series of six current pulses, with the five time intervals between the pulses changed according to the data. The time between pulses may be either 3.15ms, representing a ONE, or 2.1ms, representing a ZERO. These times are in the ratio 3:2, with the pulse width being about one sixth of the ZERO time, ie 350us. The 5-bit key code consists of a ONE followed by the 4-bit key code shown in the table below. Key codes are transmitted continuously, with a gap of about twice the ONE time between each code word.

An example is given for the key 6 (code = 0 0 1 0):-



Key	Data code			
	D3	D2	D1	D0
No key pressed	No data pulses			
0	0	1	0	0
1	1	0	1	1
2	0	1	1	1
3	0	0	1	1
4	1	0	1	0
5	0	1	1	0
6	0	0	1	0
7	1	0	0	1
8	0	1	0	1
9	0	0	0	1
Cancel (*)	1	0	0	0
Enter (#)	0	0	0	0

3.6 Test routines.

A small part of the control program is devoted to test and alignment routines. These check for the correct operation of parts of the control system and provide signals and receiver states convenient for testing and aligning the receiver. The control system tests are not exhaustive, and the fact that the test routines do not report an error should not be used as verification of a faultless unit, but many errors can be detected, and often the type of fault reported is a useful guide to repair.

In test mode the five buttons on the front panel serve to control the program. For convenience these are designated **TEST1** through to **TEST5** (ie **MEMORY SELECT** is **TEST1** and **MHz UP** is **TEST5**). The receiver is set into test mode by depressing the **TEST1** button as it is switched on, and the message **TEST** should appear on the display. This message will remain on the display provided that no faults are found, if a fault condition is detected the display changes to show the **FLT** message. To clear a fault indication the receiver must be switched off.

For instructions on how to use the test routines for checking and alignment, please refer to the **Test and alignment** section of this manual. Here, the testing procedures used by the program are outlined.

When the receiver is switched on, in normal mode or test mode, a brief check is performed on the program memory and microprocessor registers. A failure in this test will result in a fault indication immediately and the receiver will not operate. The remaining tests are initiated by pressing one of the **TEST** buttons. Most tests will operate continuously whilst a **TEST** button is held, allowing serial data lines to be monitored with test equipment.

TEST1 Enters TEST mode from switch-on, and sends test message to display.

TEST2 Programmes and tests the frequency memory RAM chip. Note that any frequencies saved will be lost when this test is executed. A fault indication will result if and data corruption is detected. The frequencies stored in the memory can be later used to test filter and oscillator switching (see below).

TEST3 Programmes the receiver control registers for alignment phase 1 (see below).

TEST4 Programmes the receiver control registers for alignment phase 2 (see below).

TEST5 Returns to normal receiver operating mode (end of test sequences).

Alignment frequencies entered in RAM by TEST2 :-

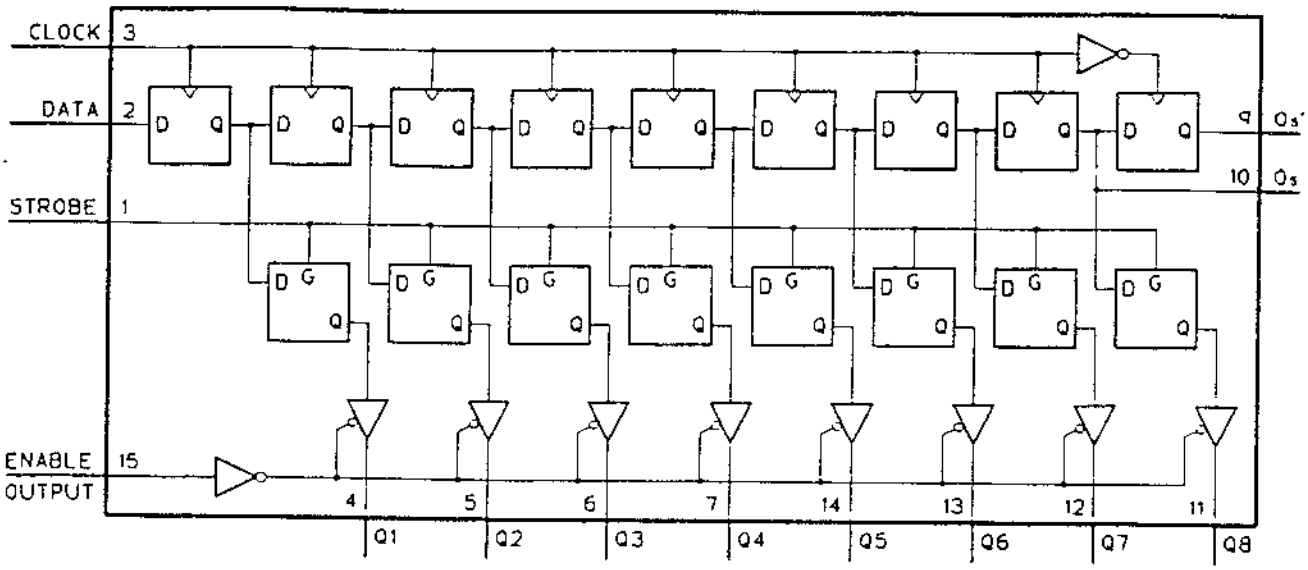
Memory number	Frequency	Purpose
1	29.900 MHz	HF LO adjust, Input filter 6 check
2	19.000 MHz	Local osc range 2 to 3 switching
3	11.000 MHz	Local osc range 1 to 2 switching
4	5.000 MHz	Local osc range 0 to 1 switching
5	100 kHz	Low frequency LO check
6	500 kHz	Input filter 1 and 2 check
7	1.700 MHz	Input filter 2 and 3 check
8	4.200 MHz	Input filter 3 and 4 check
9	11.000 MHz	Input filter 4 and 5 check
10	19.000 MHz	Input filter 5 and 6 check
VFO and all other memories	14.000 MHz	

Receiver state set by TEST3 and TEST4 :-

Control function	TEST3 state	TEST4 state
LO range select	Range 0	Range 0
PLL system	LO frequ = 45.000 MHz	LO frequ = 44.999 MHz
HET oscillator	Data = 0 0 0 0 0 0 0 0	Data = 1 1 1 1 1 1 1 1
	HET frequ = 44.545 MHz	HET frequ = 44.544008 MHz
Input filter select	No filters selected	No filters selected
IF bandwidth select	7 kHz	7 kHz
AF filter select	Normal (wide)	Normal (wide)
FM squelch control	Squelch bypassed	Squelch bypassed
RF attenuator	Out (but both relays off)	Out (but both relays off)

Semiconductor data.

74HC4094 Shift and store bus register, Q13, Q14, Q30 and Q31.



The 4094 consists of an 8-bit shift register, transparent latch and tri-state output buffer. The shift register is loaded serially on the positive edge of each CLOCK pulse. Serial data from the last stage of the register is presented at the Os output, and, delayed until the negative edge of the CLOCK, on the Os' output. (Os' is used for cascading several registers).

Parallel data from the shift register is transferred to the latch when the STROBE line is high, and retained while STROBE is low, so the outputs are unaffected by shift register activity. The outputs are buffered with tri-state devices, but in the HF-225 these are permanently enabled.

Q13 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	Strobe	In	L [H]	RCS, pulses high at end of tune	9	Os	Out	L / H	No connection
2	Data	In	L / H	Serial data, changes during tune	10	Os'	Out	L / H	Serial data, changes during tune
3	Clock	In	H [L]	CLK, pulses low during tuning	11	Q8	Out	L / H	RFATN, high for attenuator
4	Q1	Out	L / H	FMS, high to bypass FM squelch	12	Q7	Out	L / H	IF1, high to select 500 kHz LPF
5	Q2	Out	L / H	AFF, high for narrow CW filter	13	Q6	Out	L / H	IF2, high to select 7 kHz filter
6	Q3	Out	L / H	IF5, complement of IF4	14	Q5	Out	L / H	IF3, high to select 2.2 kHz filter
7	Q4	Out	L / H	IF4, high to select 4 kHz filter	15	EO	In	H	Always high
8	Vss		L	Ground	16	Vdd		H	5V supply

Q14 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	Strobe	In	L [H]	RCS, pulses high at end of tune	9	Os	Out	L / H	No connection
2	Data	In	L / H	Serial data, changes during tune	10	Os'	Out	L / H	No connection
3	Clock	In	H [L]	CLK, pulses low during tuning	11	Q8	Out	L / H	FLT1, high for input filter 1
4	Q1	Out	L / H	/RFATN, low for attenuator	12	Q7	Out	L / H	FLT2, high for input filter 2
5	Q2	Out	L / H	LO1, high for LO range 1	13	Q6	Out	L / H	FLT3, high for input filter 3
6	Q3	Out	L / H	FLT6 / LO3, high for filter 6	14	Q5	Out	L / H	FLT4, high for input filter 4
7	Q4	Out	L / H	FLT5 / LO2, high for filter 5	15	EO	In	H	Always high
8	Vss		L	Ground	16	Vdd		H	5V supply

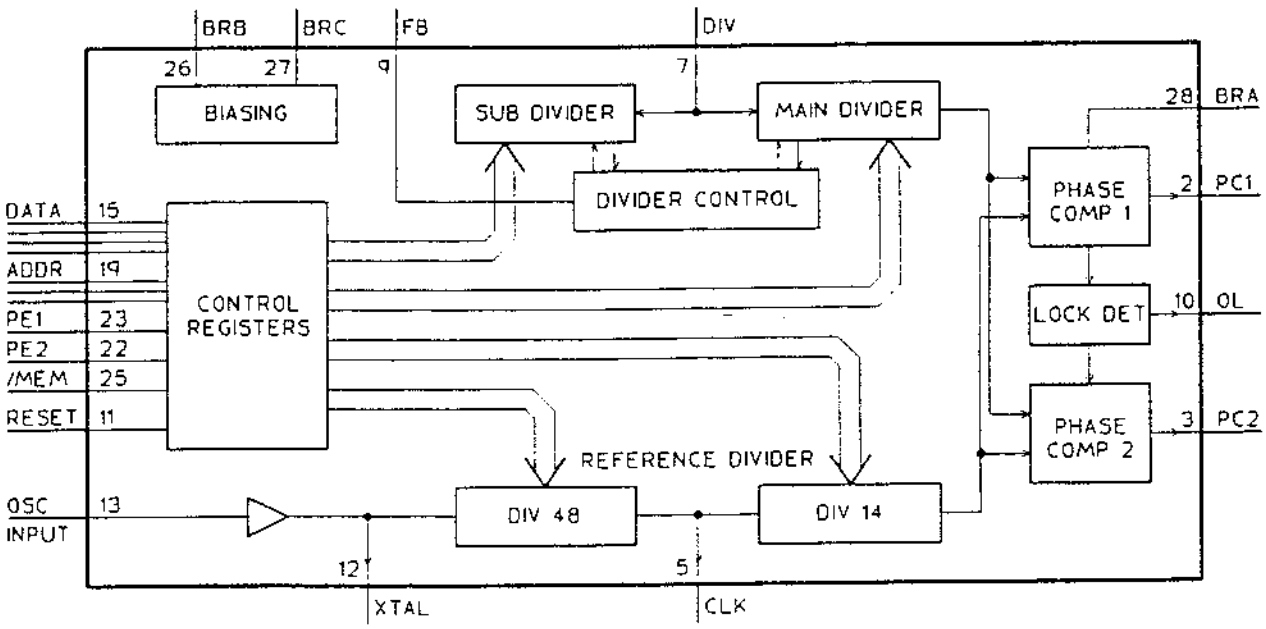
Q30 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	Strobe	In	L [H]	Pulses high at end of tune	9	Os	Out	L / H	No connection
2	Data	In	L / H	Serial data, changes during tune	10	Os'	Out	L / H	Serial data, changes during tune
3	Clock	In	H [L]	CLK, pulses low during tuning	11	Q8	Out	L [H]	Reg load, pulses when filters change
4	Q1	Out	L / H	HET0, Het osc tune bit 0	12	Q7	Out	L / H	HET6, Het osc tune bit 6
5	Q2	Out	L / H	HET1, Het osc tune bit 1	13	Q6	Out	L / H	HET5, Het osc tune bit 5
6	Q3	Out	L / H	HET2, Het osc tune bit 2	14	Q5	Out	L / H	HET4, Het osc tune bit 4
7	Q4	Out	L / H	HET3, Het osc tune bit 3	15	EO	In	H	Always high
8	Vss		L	Ground	16	Vdd		H	5V supply

Q31 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	Strobe	In	H	Always high	9	Os	Out	L / H	No connection
2	Data	In	L [H]	DATA, pulses high during tune	10	Os'	Out	L / H	Serial data, changes during tuning
3	Clock	In	H [L]	CLK, pulses low during tuning	11	Q8	Out	H [L]	PLL D0, pulses low during tuning
4	Q1	Out	L [H]	Reg load, pulses high during tune	12	Q7	Out	L [H]	PLL D1, pulses high during tuning
5	Q2	Out	L [H]	PLL A2, pulses high during tuning	13	Q6	Out	L [H]	PLL D2, pulses high during tuning
6	Q3	Out	L [H]	PLL A1, pulses high during tuning	14	Q5	Out	L [H]	PLL D3, pulses high during tuning
7	Q4	Out	L [H]	PLL A0, pulses high during tuning	15	EO	In	H	Always high
8	Vss		L	Ground	16	Vdd		H	5V supply

TDD1742T PLL frequency synthesizer, Q29.



The TDD1742D contains two programmable dividers, two phase comparators and associated logic and control circuits. The reference divider is permanently programmed to divide by 672 in the HF-225, with an intermediate tap after division by 48 giving a 14 kHz CLK signal. The main local osc divider is configured as a 13-bit binary counter, with a 4-bit sub-counter controlling the dual-modulus prescaler Q28 via the FB output.

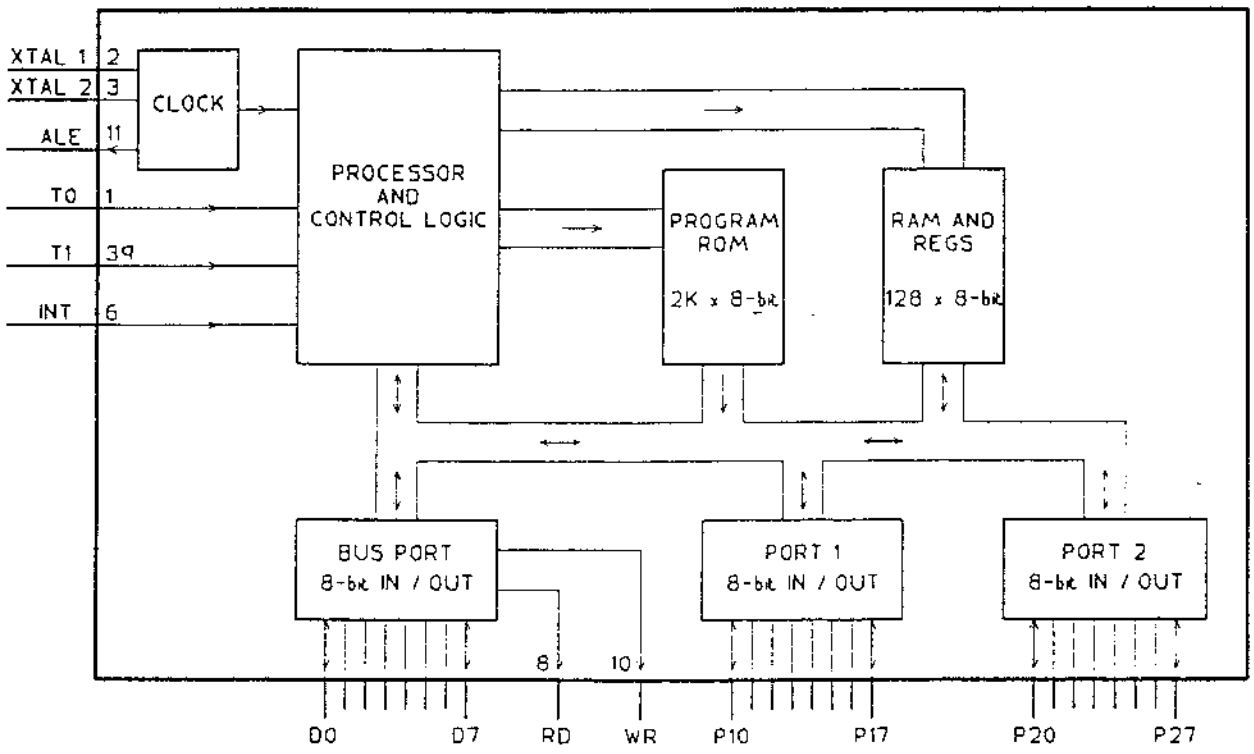
Phase comparator 1 is an analogue phase detector, consisting of a ramp generator and a sample-and-hold amplifier. Whilst the sampling point is within the linear region of the ramp only this phase detector operates, but when its linear range is exceeded digital phase comparator 2 is enabled, and the OL (out of lock) output goes high.

The functions of Q29 are controlled by 8 internal 4-bit registers. These are loaded from the receiver's microcontroller through a 4-bit DATA bus, with register selection on the 3-bit ADDR bus. Input lines PE1, PE2 and /MEM select and control this mode of operation.

Q29 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	Vdd3		8V	8V Supply	15	DB3	In	L [H]	PLL D3, pulses high during tuning
2	PC1	Out	4V	Phase comparator 1 output	16	DB2	In	L [H]	PLL D2, pulses high during tuning
3	PC2	Out	4V	Phase comparator 2 output	17	DB1	In	L [H]	PLL D1, pulses high during tuning
4				No connection	18	DB0	In	H [L]	PLL D0, pulses low during tuning
5	CLK	Out	SIG	14 kHz CLOCK output, 8Vp-p	19	AD0	In	L [H]	PLL A0, pulses high during tuning
6	Vss		L	Ground	20	AD1	In	L [H]	PLL A1, pulses high during tuning
7	DIV	In	SIG	LO in, 3-5 MHz, 1Vp-p on 3.5V	21	AD2	In	L [H]	PLL A2, pulses high during tuning
8	Vdd2		H	5V Supply	22	PE2	In	L	Always low
9	FB	Out	SIG	Psc control, narrow low pulses	23	PE1	In	L [H]	STRB, Pulses high during tuning
10	OL	Out	L	Out - of - lock output	24	MOD			No connection
11	RESET	In	L	Reset, pulses high at switch-on	25	/MEM	In	L	Always low
12	XTAL	Out	SIG	672 kHz ref signal, no connection	26	BRB			No connection
13	OSC	In		672 kHz ref input, 2Vp-p on 4.5V	27	BRC	In	4.8V	Bias current
14	Vdd1		8V	8V Supply	28	BRA	In	6.2V	Bias current

D8749H Microcontroller, Q205.



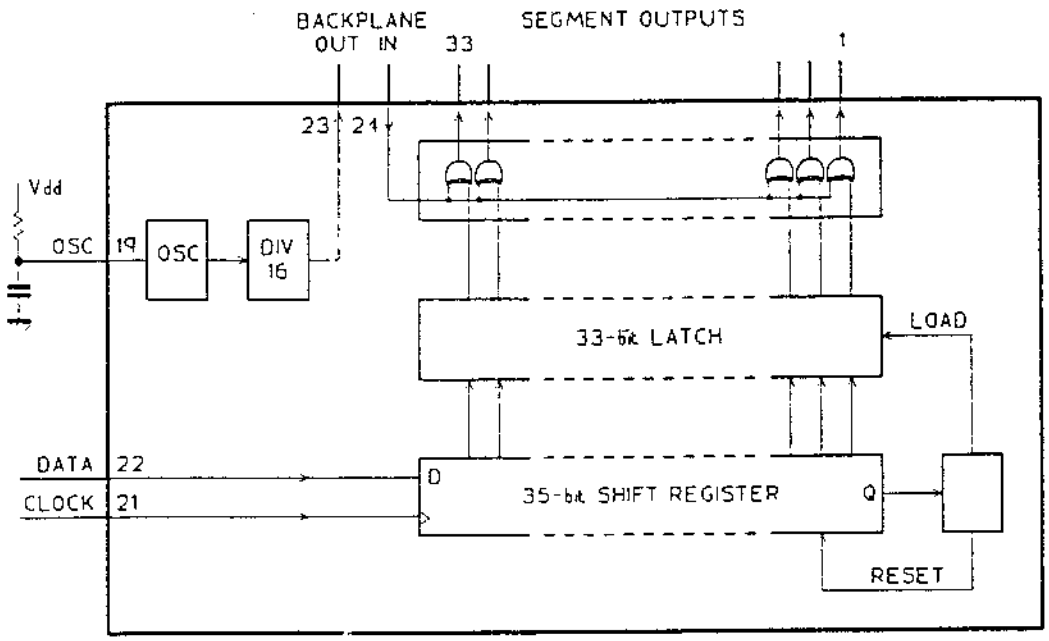
The D8749H contains all of the parts of the microprocessor control system within the HF-225. All input and output is done via three 8-bit ports, and no microprocessor bus signals come out of the chip. The ports can be configured for input or output - in the HF-225 the BUS PORT and PORT 2 are used only for output, PORT 1 is used only for input. The input ports have internal pull-up resistors to Vcc.

The on-chip clock oscillator is used with a 10.080 MHz crystal as the receiver's main reference oscillator. The ALE output is derived from this oscillator through a divide-by-15 counter.

Q205 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	T0	In	L / H	Mode, high for CW, LSB and USB	21	P20	I/O	H [L]	RAM data bit 0 and keypad data
2	XTL1	In	SIG	Crystal osc input	22	P21	I/O	H [L]	RAM data bit 1
3	XTL2	Out	SIG	Crystal osc, 3Vp-p, 10 MHz	23	P22	I/O	H [L]	RAM data bit 2
4	/RES	In	H	Reset input, low at switch-on	24	P23	I/O	H [L]	RAM data bit 3
5	/SS	In	H	Always high	25	PROG	Out	H	No connection
6	/INT	In	L / H	Mode input, high for CW and AM	26	Vdd		H	5V Supply
7	EA	In	L	Always low	27	P10	In	H [L]	MEMORY SELECT button
8	/RD	Out	H [L]	RAM /WR, pulses for RAM write	28	P11	In	H [L]	RF ATTEN button
9	/PSEN	Out	H	No connection	29	P12	In	H [L]	FILTER SELECT button
10	/WR	Out	H [L]	CLK, pulses low during tuning	30	P13	In	H [L]	MHz DOWN button
11	ALE	Out	SIG	672 kHz REF signal, 3Vp-p	31	P14	In	H [L]	MHz UP button
12	DB0	Out	L [H]	External RAM address, bit 0	32	P15	In	L / H	Low if JP1 linked
13	DB1	Out	H [L]	External RAM address, bit 1	33	P16	In	L / H	Tuning encoder phase A
14	DB2	Out	H [L]	External RAM address, bit 2	34	P17	In	L / H	Tuning encoder phase B
15	DB3	Out	L [H]	External RAM address, bit 3	35	P24	Out	L [H]	Display driver data
16	DB4	Out	L [H]	External RAM address, bit 4	36	P25	Out	H [L]	RAM /RD, low for mem recall etc
17	DB5	Out	L [H]	External RAM address, bit 5	37	P26	Out	L [H]	STRB, pulses high during tuning
18	DB6	Out	L [H]	External RAM address, bit 6	38	P27	Out	L / H	DATA, changes during tuning
19	DB7	Out	L [H]	External RAM address, bit 7	39	T1	In	L / H	Mode input, high for USB and AMS
20	Vss		L	Ground	40	Vcc		H	5V Supply

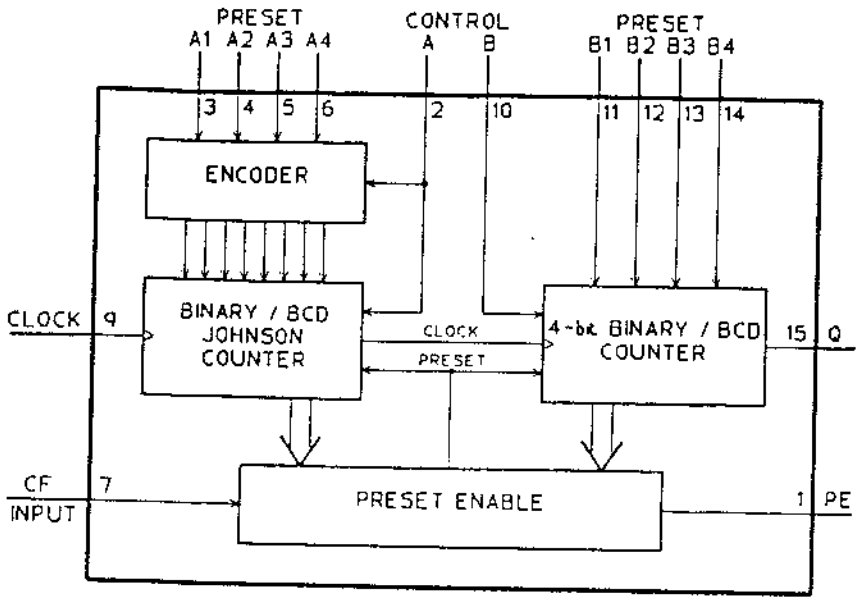
MM5453N Liquid crystal display driver, Q206.



LCD driver MM5453N contains a 35-bit shift register, 33-bit data latch, LCD driver buffers and a backplane signal oscillator. The data latches are loaded when a ONE bit is sent through the shift register. After the latches are loaded the shift register is also cleared, so new data has to pass through the entire length of the register before the latches are reloaded.

The on-chip oscillator feeds a divide by 16 counter which produces the LCD backplane signal with a 50 : 50 mark space ratio at about 60 Hz. The output drivers for each segment produce the same signal in either true or inverted form. All LCD signals swing between Ground and Vdd at 5V.

MC14569BCP Programmable divider, Q209.



The MC14569 contains two 4-bit BCD / binary down-counters that are preset from eight external inputs when the count reaches zero. In the HF-225 the chip is configured to work as a single 8-bit programmable divider. Each time the counter is preset, a pulse one clock cycle wide is produced on the PE output, this signal therefore contains many high-order harmonics of the divider output frequency. The counter is only operated when the receiver is in SSB or CW mode.

Q209 pin functions.

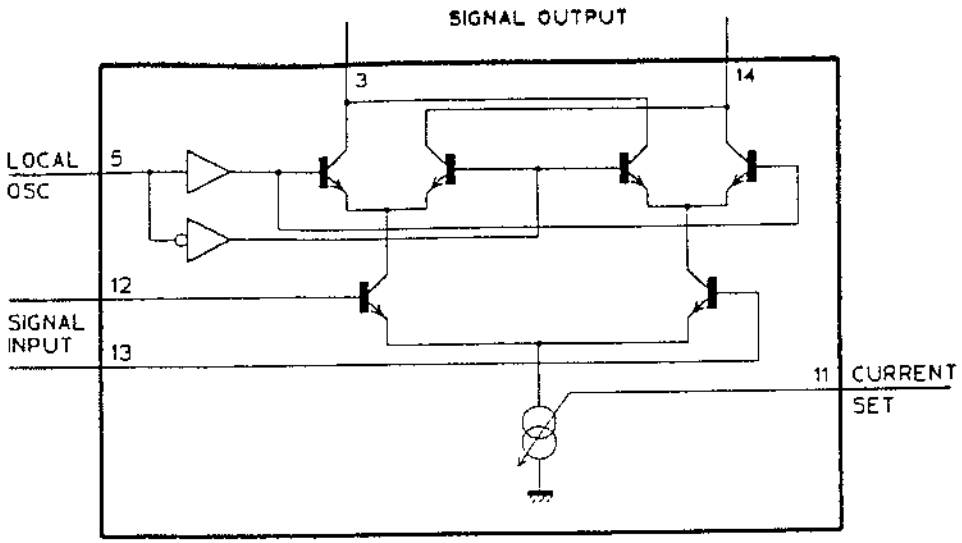
Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	PE	Out	SIG	Counter output (see section 2.1)	9	Clock	In	SIG	2.52 MHz clock
2	CtrlA	In	L	Always low	10	CtrlB	In	L	Always low
3	PR0	In	L	Preset bit 0, always low	11	PR4	In	H	Preset bit 4, always high
4	PR1	In	H	Preset bit 1, always high	12	PR5	In	L / H	Preset bit 5, low for CW
5	PR2	In	L / H	Preset bit 2, high for USB	13	PR6	In	H	Preset bit 6, always high
6	PR3	In	L / H	Preset bit 3, low for CW	14	PR7	In	H	Preset bit 7, always high
7	CF	In	H	Always high	15	Q	Out	SIG	No connection
8	Vss		L	Ground	16	Vdd		H	5V supply

SL6440CDP High level mixer, Q1 and Q2 (and Q5 in D-225).

The SL6440 integrated circuit, double-balanced mixer combines good strong signal performance and low noise. The mixer has balanced inputs and outputs, but either may be used unbalanced; in the HF-225 two configurations are found. Q1, the first mixer, uses balanced inputs and outputs to obtain maximum gain and lowest noise and distortion. The other two applications use the chip with single, unbalanced input and output lines.

The mixer performance can be adjusted by an external current source into the IP pin, and the best balance of noise, intermodulation and supply current drain can be set. An amplifier for the local oscillator signal is included on the mixer chip.

Pins 1, 2, 7, 8, 9, 10, 15 and 16 are used for thermal bonding only, and are not connected within the mixer IC. In the HF-225 they are bonded to the PCB ground plane.



Q1 pin functions.

Pin	Name	DC Voltage	Signal	Function
3	Output A	10.9V	Some LO (<50 mV)	45 MHz IF output
4	Vcc	7.8V	None	Mixer supply
5	LO in	2.0V	LO 1Vp-p	45 to 75 MHz local oscillator input
6	0V	0V	None	Ground connection
11	IP	2.7V	None	Current program input
12	Input B	5.3V	Slight LO (<10 mV)	RF signal input
13	Input A	5.3V	Slight LO (<10 mV)	RF signal input
14	Output B	10.9V	Some LO (<50 mV)	45 MHz IF output

Q2 pin functions.

Pin	Name	DC Voltage	Signal	Function
3	Output A	7.5V	Some HET (<20 mV)	Unused output
4	Vcc	6.0V	None	Mixer supply
5	LO in	2.1V	HET 400mVp-p	44.545 MHz heterodyne oscillator input
6	0V	0V	None	Ground connection
11	IP	1.6V	None	Current program input
12	Input B	3.9V	None	Unused input
13	Input A	3.9V	Slight HET (<5 mV)	45 MHz IF input
14	Output B	7.5V	Some HET (<20 mV)	455 kHz IF output

Q5 in D-225 pin functions. (Receiver in AMS mode)

Pin	Name	DC Voltage	Signal	Function
3	Output A	7.6V	Audio + 910 kHz	Unused output
4	Vcc	6.1V	None	Mixer supply
5	LO in	2.1V	455 kHz 100mVp-p	Synchronised oscillator input
6	0V	0V	None	Ground connection
11	IP	1.6V	None	Current program input
12	Input B	4.0V	455 kHz 150mVp-p	455 kHz IF signal input
13	Input A	4.0V	None	Unused input
14	Output B	7.6V	Audio + 910 kHz	AMS audio output 200mVp-p